REMARKS

Claim 1 has been amended in order to more particularly point out, and distinctly claim the subject matter to which the applicant regards as his invention. The applicant respectfully submits that no new matter has been added. It is believed that this Amendment is fully responsive to the Office Action dated May 9, 2001.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached pages are captioned "**Version with markings to show changes made**."

With respect to the Examiner's comments on Figures 3A, 3B, 4, 5 and 7, the applicant respectfully submits herewith proposed drawing corrections to Figures 3A, 3B, 4, 5 and 7, marked in red ink. The applicant respectfully requests that the proposed drawing corrections submitted herewith be approved by the Examiner.

As a result of the Response to Restriction Requirement filed April 23, 2001, claims 1 - 7 are currently pending in this application.

Claims 1 - 7 stand rejected under 35 USC §112, second paragraph, for the specific reasons set forth in item 5, page 3 of the outstanding Action.

Here, the applicant has deleted the phrase "toward an interior of said substrate" from the last clause of claim 1.

As such, the outstanding indefiniteness rejection is now moot. Accordingly, the withdrawal of the outstanding indefiniteness rejection under 35 USC §112, second paragraph, is in order, and is therefore respectfully solicited.

As to the merits of this case, the following rejections are set forth:

(1) claims 1 - 6 stand rejected under 35 USC§103(a) based on Iwase (Japanese Patent Publication No. 7-201855) in view of the "Admitted Prior Art" (APA); and

(2) claim 7 stands rejected under 35 USC §103(a) based on Iwase and APA, and further in view of Japanese Patent Publication No. 10-335456.

The applicant respectfully requests reconsideration of these rejections.

As set forth in lines 21 - 26, page 8 of the applicant's specification, the object of the applicant's present invention is to provide a semiconductor device having a guard ring structure, wherein the problem of exfoliation of the guard ring structure during a CMP process is effectively eliminated. In order to achieve this object, the present invention is directed to a zigzag pattern of one of a triangular wave pattern and a rectangular wave pattern for the guard ring, as now set forth in amended claim 1.

By using the guard ring pattern as set forth in amended claim 1, the problem of damaging the guard ring pattern at the time of the CMP process is effectively eliminated.

Contrary to the teachings of the applicant's instant claimed invention, the pattern of Iwase is designed for reducing the stress caused during the molding process. In the paragraph [003]of Iwase, it is clearly described that the strong stress caused by the molding resin is applied to four corners 9 at the periphery of the semiconductor chip, resulting in a cracking in the passivation film covering the conductive film 3 of the guard ring 4.

As explained with reference to the applicant's Figures 3 and 4, stress is applied in one direction in the case of the CMP process. Thus, there is no motivation to a person of ordinary skill in the art to use Iwase's pattern in a multilayer interconnection structure as in the "Admitted Prior Art."

In order to further structurally distinguish the applicant's instant claimed invention, the applicant has incorporated into independent claim 1, as filed herewith, the structural arrangement of the guard ring pattern having one of a triangular wave pattern and a rectangular wave pattern.

Further, the applicant has incorporated into independent claim 1, as filed herewith, the structural arrangement whereby the guard ring pattern is formed by a CMP process.

The limited teachings of the Japanese Patent Publication No.10-335456 do not supplement the teachings of the above-discussed references in failing to fully meet the applicant's claimed invention, as now set forth in amended claim 1.

In view of the above, the applicant respectfully submits that the teachings of the cited prior art references fail to teach the above-discussed distinguishable claimed structural arrangements, as now set forth in amended independent claim 1 filed herewith. As such, even if, *arguendo*, the teachings of the cited references can be combined in the manner suggested by the Examiner, such combined teachings would still fall far short in fully meeting the applicant's claimed semiconductor device, as now set forth in amended independent claim 1. Accordingly, a person of ordinary skill in the art would not have found the applicant's claimed invention, as now set forth in amended claim 1 filed herewith, obvious under 35 USC§103(a) based on the teachings of the cited prior art references, singly or in combination.

In view of the above, the withdrawal of the outstanding obviousness rejection under 35 USC§103(a) based on Iwase (Japanese Patent Publication No. 7-201855) in view of the "Admitted Prior Art" (APA), and the outstanding obviousness rejection under 35 USC §103(a) based on Iwase and APA, and further in view of Japanese Patent Publication No. 10-335456 is in order, and is therefore respectfully solicited.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact the applicant's undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, the applicant respectfully petitions for an appropriate extension of time. The fees for such an extension or any other fees which may be due with respect to this paper, may be charged to Deposit Account No. 01-2340.

Respectfully submitted,

ARMSTRONG, WESTERMAN, HATTORI,
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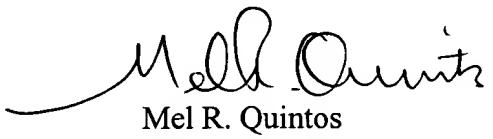

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Enclosures: (1) Version with markings to show changes made
(2) Petition for Extension of Time
(3) Request for Approval of Drawing Corrections

VERSION WITH MARKINGS TO SHOW CHANGES MADE (09/528,296)

IN THE CLAIMS:

Please amend claim 1 as follows:

1. (Amended) A semiconductor device, comprising:

a substrate; and

a multilayer interconnection structure formed on said substrate,

said multilayer interconnection structure including: at least first and second interlayer insulation films provided on said substrate; and a guard ring pattern embedded in each of said first and second interlayer insulation films, said guard ring pattern extending along a periphery of said substrate, said multilayer interconnection structure being planarized by using a CMP process,

wherein said guard ring pattern changes a direction thereof repeatedly and alternately in a plane parallel to said substrate,

said guard ring pattern including: a conductive wall extending in each of said first and second interlayer insulation films from a bottom principal surface thereof to a top principal surface thereof; and a conductive pattern making a contact with a top part of said conductive wall and having a principal surface coincident to said top principal surface of said interlayer insulation film, said conductive wall changing a direction thereof repeatedly and alternately in one of a triangular wave pattern and a rectangular wave pattern in said plane in correspondence to said guard ring pattern,

said conductive wall in said first interlayer insulation film being offset with respect to said conductive wall in said second interlayer insulation film in a direction parallel to a principal surface of said substrate [toward an interior of said substrate] when viewed in a direction perpendicular to said principal surface of said substrate.